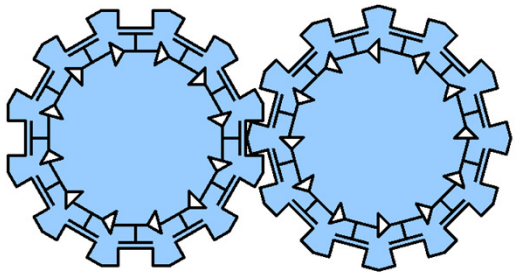


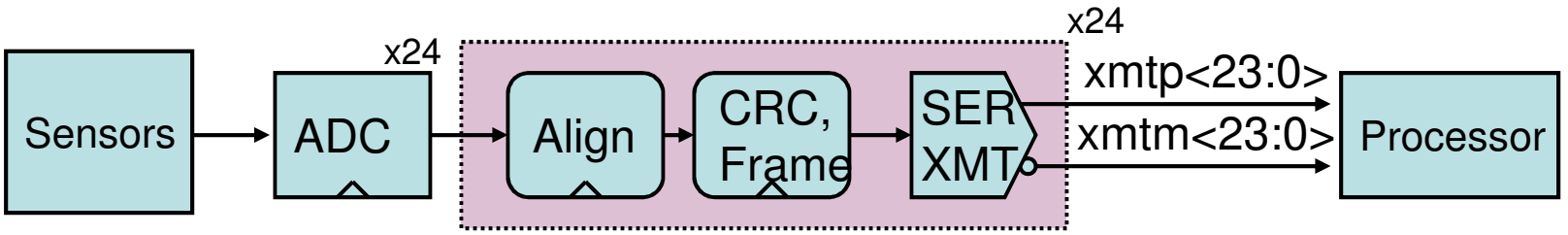
Efficient Gbit/s Data Transceivers Designed for Verification and SoC Integration

Bill Ellersick

Analog Circuit Works

Introduction

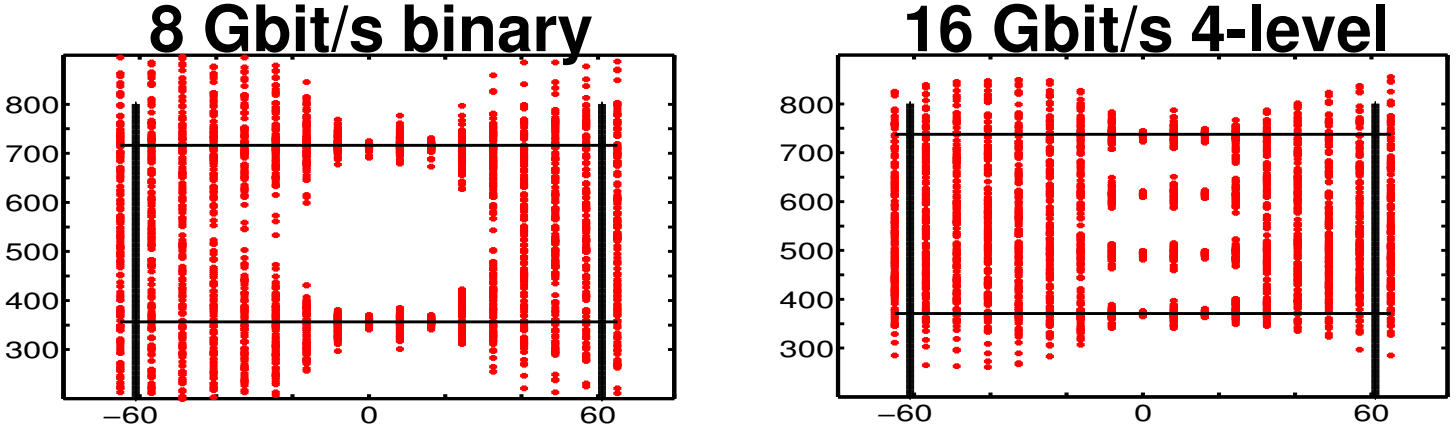
- Secure embedded systems: trusted design



- HPEC -> Tbit/s between chips on wires/fibers
- SERDES Research: tens of Gbit/s/link
- Practical electrical interfaces: 3-10 Gbit/s/link
  - Sweet spot for circuit complexity, power, area
  - Advances in packaging: highly parallel links
  - Power and area per Gbit/s can trump Gbit/s/link

Mature SERDES Architecture

- Proven transceiver design
  - Design optimized over 5 successful tapeouts
  - Focus: cost, robustness, time-to-market
- Based on 16 Gbit/s 0.25um link: 69mW/Gbit/s, 3mm^2
  - Calibration, linear equalization + DFE, 4-PAM, 0.25um [1]

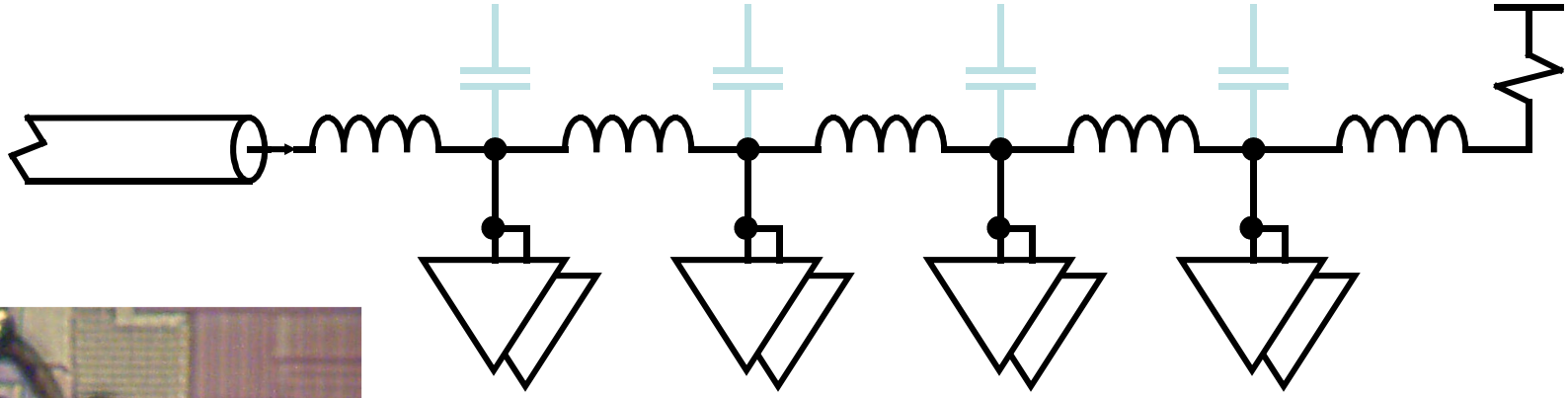


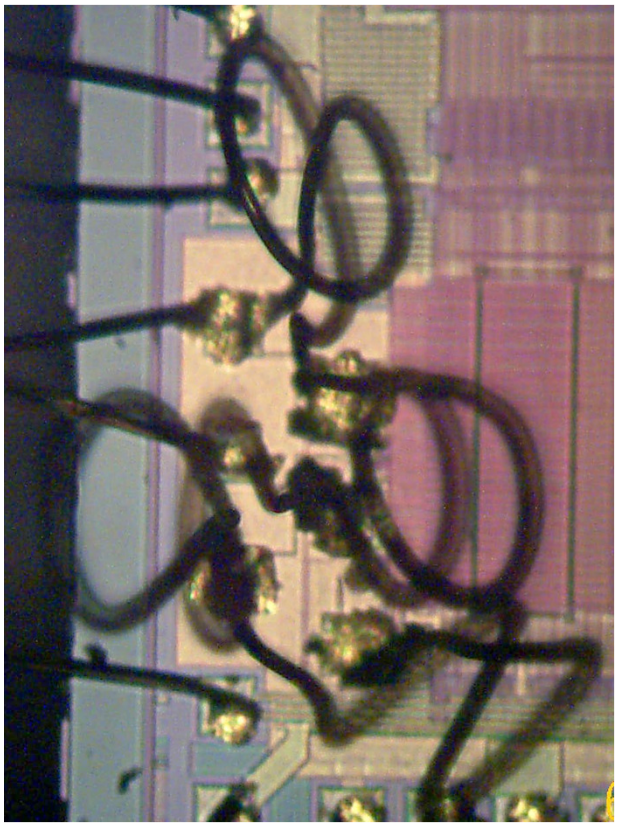
- Performance scales w/process, 2mW/Gbit/s, .02mm^2
  - Simple linear equalization, fits under SERDES pads

Outline

- Introduction
- Complex 16 Gbit/s SERDES
- Simple, practical SERDES architecture
  - Coding/Scrambling, Clock Recovery
  - Equalization
  - Standards
- Real value behavioral models
- Integration into SoCs
- Conclusion

16 Gbit/s in 0.25um: inductive tuning

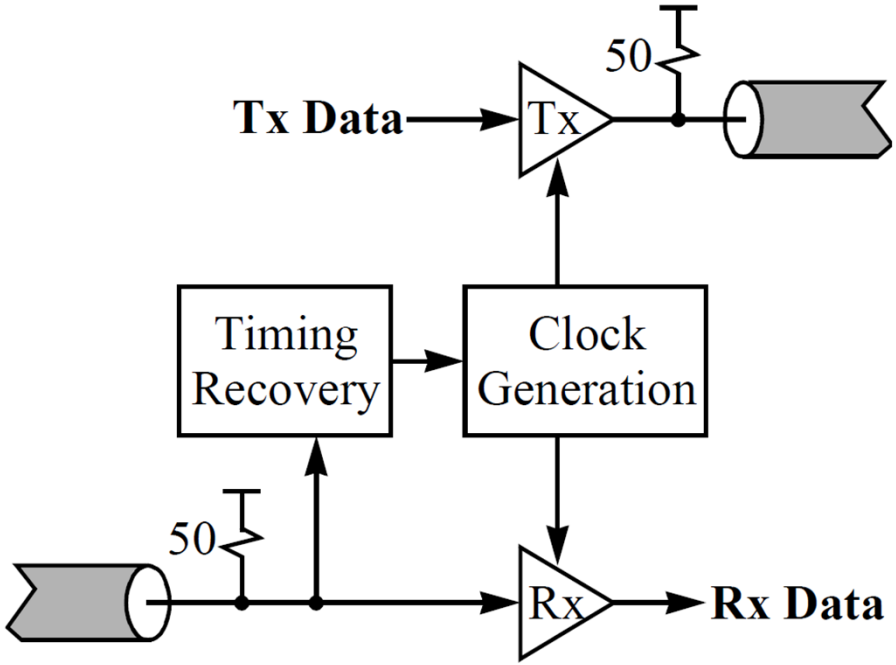




- Bond wire inductors for low Q
- Time interleaved transceivers
  - Parallelism, needs calibration
- Extreme limits of Gbit/s/link
- 4-PAM to lower symbol rate
- Simpler: 2-PAM, lower Gbit/s
  - More parallel wires

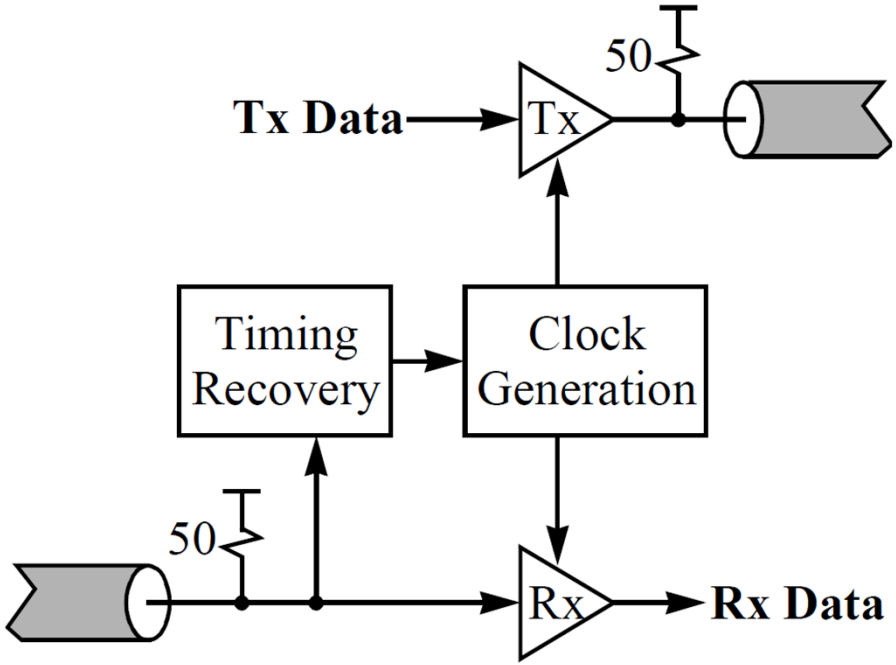
Link Architecture

- Links constructed from mixed-signal blocks
  - PLL, Tx, Rx, Timing Recovery
- Synthesized logic for coding, upper layers
- Double termination: high BW, small reflections



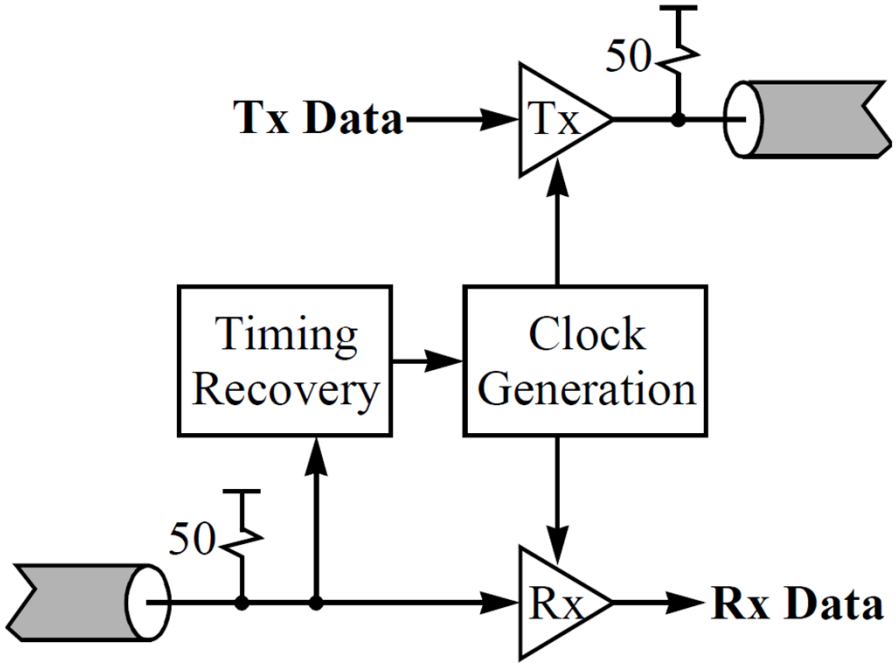
Coding/Scrambling

- Embedded clocks for high data rates
- Low overhead coding: edges, DC balance
  - Prevent long series of zeros or ones
  - Self-synchronizing scramblers (per SONET)
  - 8B10B or 32B34B (complicates clock dividers)



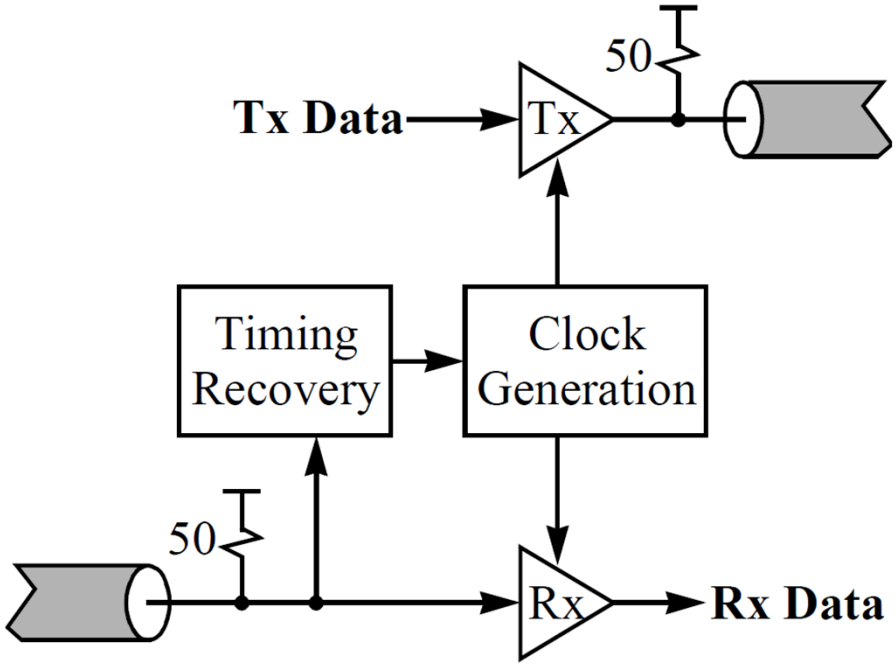
Clock Recovery

- Digital clock recovery: predictable, scalable
  - Robust phase synthesizers adjust clock phases
  - Digital state machines align clocks to rx data
  - Compensates for phase, small freq. differences



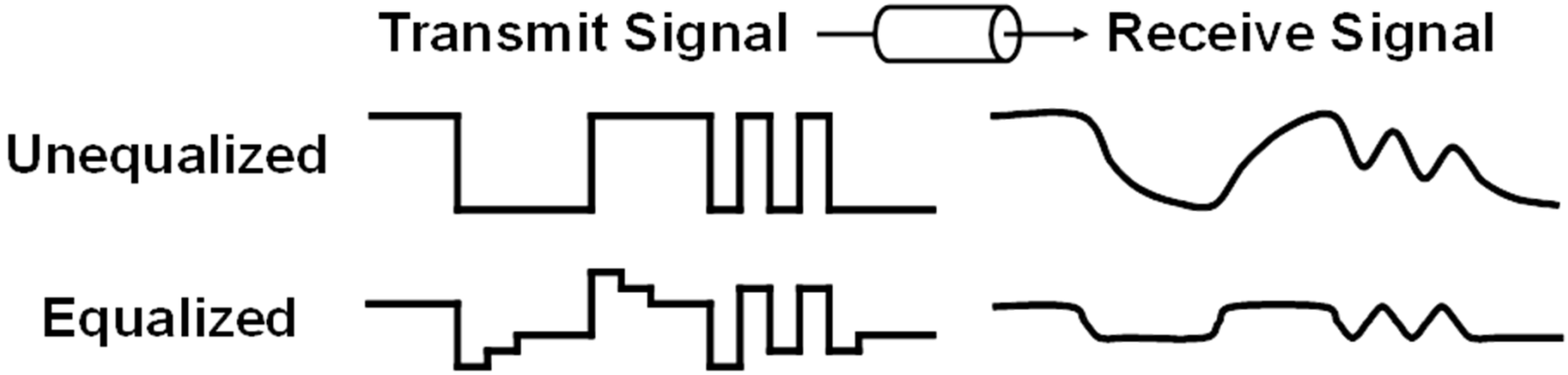
Clock Generation and Retiming

- One PLL
  - Generates clocks for multiple SERDES
  - Filters out high frequency jitter (eases shielding)
  - Duty cycle correcting clock buffers
- Retiming flip-flops in SERDES eases timing



Equalization

- Linear equalization preferred (Tx equ. shown below)
  - Emphasizes high frequency edges
  - Easily verified eye openings, good until near Gbit/s limit
  - Slightly larger signal swings vs. DFE (lower SNR)
  - Coefficients fixed (adapted if application allows)
- Unrolled DFE[1] complex and power-hungry
- Real-time DFE hard to port, power-hungry



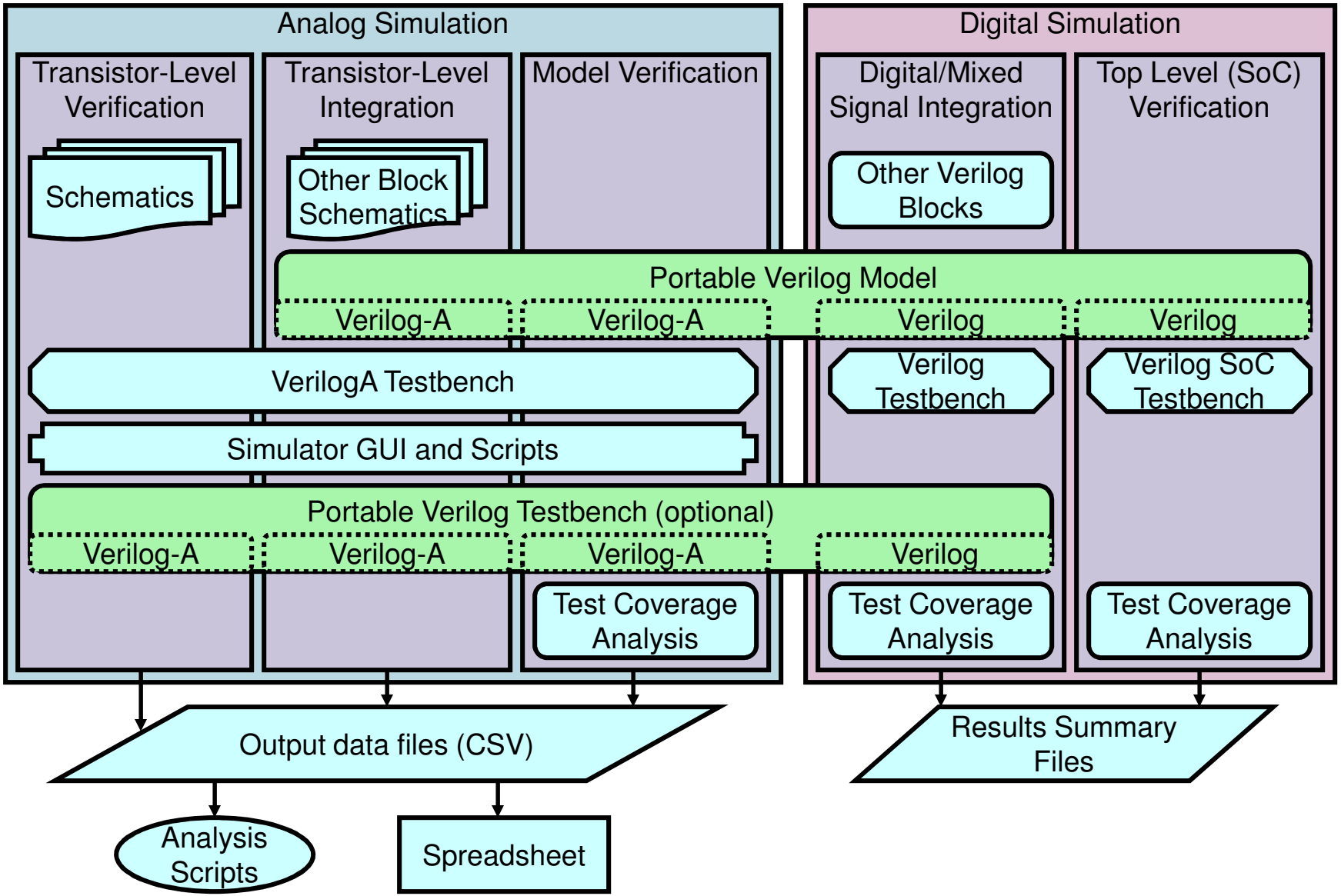
Lean SERDES vs. Standards

- One Configurable PHY for multiple standards
  - JESD, PCIe, XAUI, Thunderbolt, 10GbE, USB3.0
  - Upper layers in synthesizable macros
- Internal system links: lean protocol stack
  - Simple coding or scrambling
  - Provides framing and edges for clock recovery

Real Portable Models

- Accurate models of SERDES for SoC design
- EDA tools now widely support Verilog standards
- Real Portable Methodology
  - Portable across processes and tools
  - Rapid discrete-time real-valued behavioral simulation
    - Time honored approach: commonly used in e.g. Matlab
  - Verification of model vs. transistor-level design
  - Enhanced productivity, portable, reusable
- Can develop IP with one set of tools
  - Integrate into SoC with another set of tools
  - Benefits IP providers, users, tool providers

Real Portable Methodology Flow



SERDES Integration into SoCs

- Chip and board layout guidelines
  - Identify victim and aggressor signals
  - Drives floorplanning and routing
- Placement of SERDES near power/data pads
  - Noisy supply pads dictate substrate current
- Shielding or twisted differential signals
- Controlled impedance packaging, connectors
- Review by experienced SERDES designers

Conclusions

- First silicon success is paramount in SoCs
  - SERDES a fraction of power/area/design effort
- Keep it simple
  - Reuse and port building blocks
  - Optimize to sweet spot of process and application
  - Minimize cost, reduce time-to-market
  - Allows HPC with robust, efficient SERDES
- Verification, integration methods minimize risk
- Boutique process, secure embedded systems
  - Trusted, proven SERDES blocks not available

References

- [1] Ellersick, W., et al, "A Serial-Link Transceiver Based on 8-GSample/s A/D and D/A Converters in 0.25-mm CMOS", ISSCC 2001.
- [2] Ellersick, W., "Real Portable Models for System/Verilog/A/AMS", Cadence CDN Live Conference, October 2010