50% Power Reduction Through Automated Synthesis of an Asynchronous Microprocessor and Logic from Synchronous RTL

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Power-efficiency is key to mobile and datacenters
Industry is shifting from raw performance to performance per watt

REM and ACW are fabless semiconductor companies collaborating on unique technology to build ultra-efficient processors
POWER EFFICIENT MICROPROCESSOR PROJECT

- Asynchronous logic to reduce power (same functionality from outside)
- Integrated power management with 5 zones to optimize different circuit types

Legend:
- Analog
- Digital
- Interface

Synchronous µProcessor

- µProcessor
- Sync Core
- Sync Logic
- I/O
- Memory
- SERDES

Asynchronous µProcessor

- µProcessor
- Async Core
- Async Logic
- I/O
- Memory
- SERDES
- Power
- Vdd<4:0>

Sync to Async Scripts
Optimize/Verify vs. Vdd
Integrated Power Mgmt

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Synchronous designs are built around the worst-case Area and power overhead required to hit performance target can be substantial.
OVERVIEW

• Introduction
  ➢ Resilient bundled data technology
• Supply voltage scaling
• Synchronous to asynchronous EDA flow
• Summary
RESILIENT BUNDLED DATA

Static combinational logic and standard latches (or FFs)
Delay > worst-case combinational logic delay 90% of the time
10% of the time, logic outputs change after delay: hold off next stage
Resilient BD allows cycle time to change depending on input data. Assumes long data dependent cycles are rare: average performance improves.
Worst-case operations occur infrequently. Wide variability in delay shows potential to optimize designs for average case performance.
SELECTABLE DELAYS

Identify blocks with variable delay based on operation (manually)
Change delay of stage on cycle-by-cycle basis
Achieve averaging over time
AVERAGE CASE PERFORMANCE

Removing worst-case logic will cause some instructions to take longer.
On average performance does not change.
Smaller logic blocks are more power and area efficient.
Dropping voltage trades performance for power savings
Match synchronous performance at a lower voltage
INCREASED SPEED CAN INCREASE POWER EFFICIENCY EVEN MORE

- When peak speed not needed, run at lower Vdd
- Power drops faster than speed as Vdd drops => efficiency increases
  - Chart shows 28nm normalized logic efficiency (Gops/W) vs. Vdd
  - Blue curve includes efficient, integrated buck and charge pump converters
RESILIENT BD ADVANTAGES

Exploits data dependency in delay regardless of logical function enabling a more generic approach

Allows designers to cut margins as timing violations will be detected and corrected
EDA FLOW OVERVIEW

Design flow on top of existing synchronous EDA flow

Custom Tcl / Perl scripts to glue between tools and generate constraints

Benefits from advancements in synchronous IP (e.g. ARM core) & EDA tools
SYNC TO ASYNC SYNTHESIS

• Automated conversion of synchronous netlist to asynchronous
  • Choose asynchronous logic domains
  • Replace flip-flops with latches
  • Add custom cells: delay lines, error detecting latches, and control logic
INTERACTIVE OPTIMIZATION, TIMING CLOSURE

Define virtual clock for each async controller to establish constraints

Period / Delay difference between clocks based on analysis of async circuit

Async tools analyze average case performance and generate constraints
Iterate to obtain desired performance post-synthesis and post-P&R
Delay lines synthesized, modified during P&R
TECHNOLOGY SUMMARY

Smaller Logic

Less Wasted Time

Lower Voltage

Power Savings
RECENT RESULTS

• 130nm computational logic ASIC
  • Flawless operation from 0.65 to 1.3V, silicon-verified
  • 3.39M transistors in 10.35mm$^2$ with 6 power domains
  • Excellent power efficiency, matching simulation

• 28nm 3-stage OpenCore MIPS CPU
  • 14k gates
  • 15,226 um$^2$: 9% area increase vs. 14,000 um$^2$ synchronous design
  • 35% speedup vs. synchronous design
WHY RESILIENT BUNDLED DATA

- Automatic conversion from sync RTL avoids costly redesign
- Tolerates variations and recovers in realtime
  - Performance improves as supply drops (variations increase)
  - Handles rapid changes in supply voltage gracefully
- 100s of timing constraints vs. 100K in previous async flows
  - Combinational blocks are similar to synchronous combinational blocks
EDA TOOL POWER OPTIMIZATION + ASYNC TECHNOLOGY

• Commercial EDA synthesis and logic optimization
  + Synchronous to asynchronous logic flow
  + On-chip multi-zone power management
  = World-class power efficiency
SUMMARY

Building highly efficient processors

REM’s and ACW’s asynchronous technology enable average-case design and efficiency gains

Optimizing asynchronous flow with latest EDA tool advances

Looking to partner on products